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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/895,566	06/29/2001	Jun-Cheng Ko	LAM2P258	6944
25920	7590	09/12/2003		
MARTINE & PENILLA, LLP 710 LAKEWAY DRIVE SUITE 170 SUNNYVALE, CA 94085			EXAMINER	VINH, LAN
			ART UNIT	PAPER NUMBER
			1765	

DATE MAILED: 09/12/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No.	Applicant(s)
	09/895,566	KO ET AL.
Examiner	Art Unit	
Lan Vinh	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

1) Responsive to communication(s) filed on 07 July 2003.

2a) This action is FINAL. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

4) Claim(s) 1-10 and 16-21 is/are pending in the application.

4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.

5) Claim(s) \_\_\_\_\_ is/are allowed.

6) Claim(s) 1-10 and 16-21 is/are rejected.

7) Claim(s) \_\_\_\_\_ is/are objected to.

8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) The proposed drawing correction filed on \_\_\_\_\_ is: a) approved b) disapproved by the Examiner.  
If approved, corrected drawings are required in reply to this Office action.

12) The oath or declaration is objected to by the Examiner.

#### Priority under 35 U.S.C. §§ 119 and 120

13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some \* c) None of:

- Certified copies of the priority documents have been received.
- Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
- Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a)  The translation of the foreign language provisional application has been received.

15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

#### Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____	6) <input type="checkbox"/> Other: _____

## DETAILED ACTION

### ***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-8, 10, 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cain (US 5,242,532) in view of Gabriel (US 5,198,072)

Cain discloses a method of plasma endpoint detection etches a designated layer of a specified material on a substrate. This method comprises the steps of:

forming a semiconductor structure 202 having a gate member 210 on/over a surface of the substrate 206 (col 4, lines 14-20, fig. 2A), which reads on forming a gate structure on/over a first surface of the substrate

forming spacers 234 along sidewall of gate structure 210 (col 4, lines 56-57, fig. 2C)

forming source region 246 and drain diffusion region 250 in the surface of the substrate 206 (col 4, lines 65-66, fig. 2C shows that source/drain regions 246 and 250 located/defined outside of the spacer 234

forming a TEOS (tetraethylorthosilicate) layer 402 over the surface of the substrate 206 (col 7, lines 39-40), fig. 5C shows that layer 402 is formed between dielectric layer 410 (BBSG) and the substrate surface 206 and the layer 402 overlies the gate structure 210, the spacers 234 and the surface of the substrate, which reads on forming an interlevel dielectric layer (IDL) directly over the first surface of the substrate without

forming a stop layer, such that the IDL layer overlies the gate structure, the spacers and the first surface of the substrate since Cain does not disclose forming a silicon nitride layer (claimed etch stop layer as defined in page 1 of the specification) on the layer 402/dielectric layer

plasma etching through the layer 402/IDL layer, in a plasma chamber, to form an opening 242/contact hole to the top layer of gate structure 210 and an opening 250/via hole exposing the source/drain regions (col 7, lines 61-67, col 8, lines 1-2, fig. 5E)

monitoring a DC bias of the plasma etcher/plasma processing chamber during etching (col 8, lines 56-59)

generating an endpoint signal upon completing the etching step employing endpoint monitoring apparatus sensitive to parameter such as the DC bias level (col 8, lines 37-38), which reads on discontinuing the plasma etching process when detecting an endpoint signal in the DC bias

generating an endpoint signal indicating removal of the thin layer upon exposure of the substrate 306 (col 7, lines 15-18, fig. 6F shows that the surface of substrate 306 underlying the contact hole is exposed)

Unlike the instant claimed inventions as per claims 1, 6, 21, Cain does not specifically disclose the step of monitoring a bias compensation voltage (a method used to regulate the voltage present on the wafer as defined in page 14 of the specification) of the plasma processing chamber during the plasma etching and discontinue the plasma etch upon detecting a endpoint signaling change in the bias compensation voltage.

However, Gabriel discloses a method and apparatus for detecting endpoint when etching dielectric layer comprises the step of monitoring DC bias change (voltage rise /step increase) on the cathode 16/substrate (wafer) 42 to terminate the etching of the dielectric layer (col 2, lines 61-62, col 3, lines 67-68, col 4, lines 9-14, fig. 1). Gabriel teaching reads on the step of monitoring a bias compensation voltage (a method used to regulate the voltage present on the wafer as defined in page 14 of the specification) of the plasma processing chamber during the plasma etching and discontinue the plasma etch upon detecting a endpoint signaling change in the bias compensation voltage.

Since Cain discloses that plasma etcher using endpoint monitoring apparatus sensitive to parameters such as DC bias level may be used to implement the etching process (dielectric etching process) (col 8, lines 56-60), one skilled in the art would have found it obvious to modify Cain method by using the endpoint method as taught per Gabriel since Gabriel states that his invention detects imminent endpoint when plasma etching dielectrics thereby permitting the process to be terminated before the substrate is damaged (col 2, lines 58-60)

Regarding claims 2, 7, Cain discloses that the endpoint signal is generated upon completing etching (col 8, lines 37-40). Fig. 6F shows the etching exposes a portion of the surface of the substrate under the contact hole and a portion of the top layer of the gate structure.

The limitations of claims 3, 4, 5 have been discussed above.

Regarding claim 8, Cain also discloses forming a gate oxide 212 over the surface of the substrate and forming a polysilicon layer 210 over the gate oxide 212 (col 4, lines 16-17, fig. 2A)

Regarding claim 10, Cain discloses forming a spacer layer 234 over the surface of the substrate and the gate structure and plasma etching the spacer layer to form spacer 234 along the sidewall of the gate structure 210 (col 4, lines 14-20, fig. 2C)

3. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cain (US 5,242,532) in view of Gabriel (US 5,198,072) and further in view of Liaw (US 5,843,815)

Cain as modified by Gabriel has been described above in paragraph 2. Unlike the instant claimed invention as per claim 9, Cain and Gabriel do not disclose depositing an oxide layer over the first surface of the substrate, the gate structure and spacer, depositing a TEOS layer over the oxide and an oxide layer over the TEOS.

However, Liaw discloses a process for forming a MOSFET device/transistor comprises the steps of depositing an oxide layer 10 over the first surface of the substrate, the gate structure and spacer, depositing a TEOS layer 30 over the oxide and an oxide layer 19 over the TEOS (col 4, lines 17-18, col 5, lines 10-24, fig. 7)

Hence, one skilled in the art would have found it obvious to modify Cain and Gabriel by forming an insulating composite structure as per Liaw because according to Liaw a composite interlevel dielectric resulting in a smooth topology (col 5, lines 21-32)

4. Claims 16-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cain (US 5,242,532) in view of Gabriel (US 5,198,072)

Cain discloses a method of plasma endpoint detection etches a designated layer of a specified material on a substrate. This method comprises the steps of:

forming a semiconductor structure 202 having a gate member 210 on/over a surface of the substrate 206 (col 4, lines 14-20, fig. 2A), which reads on providing a substrate having a transistor structure on a surface of the substrate.

forming a TEOS (tetraethylorthosilicate) layer 402 over the surface of the substrate 206 (col 7, lines 39-40), fig. 5C shows that layer 402 is formed between dielectric layer 410 (BPSG) and the substrate surface, which reads on forming a dielectric layer directly over the first surface of the substrate without forming a stop layer since Cain does not disclose forming a silicon nitride layer (claimed etch stop layer as defined in page 1 of the specification) on the layer 402/dielectric layer

plasma etching through the layer 402/dielectric layer, in a plasma chamber, to form an opening 242/contact hole in the dielectric layer (col 7, lines 61-67, fig. 5E)

introducing reactant/etchant gases into the plasma chamber (col 6, lines 50-60)

activating the power supply to the plasma chamber strikes the plasma and activate the plasma etching process (col 2, lines 11-12)

monitoring a DC bias of the plasma etcher/plasma processing chamber during etching (col 8, lines 56-59)

generating an endpoint signal upon completing the etching step (col 8, lines 37-38), which reads on discontinuing the plasma etching process when detecting an endpoint signal.

Unlike the instant claimed inventions as per claim 16, Cain does not specifically disclose the step of monitoring a bias compensation voltage (a method used to regulate the voltage present on the wafer as defined in page 14 of the specification) of the plasma processing chamber during the plasma etching and discontinue the plasma etch upon detecting a endpoint signaling change in the bias compensation voltage.

However, Gabriel discloses a method and apparatus for detecting endpoint when etching dielectric layer comprises the step of monitoring DC bias change (voltage rise /step increase) on the cathode 16/substrate (wafer) 42 to terminate the etching of the dielectric layer (col 2, lines 61-62, col 3, lines 67-68, col 4, lines 9-14, fig. 1). Gabriel teaching reads on the step of monitoring a bias compensation voltage (a method used to regulate the voltage present on the wafer as defined in page 14 of the specification) of the plasma processing chamber during the plasma etching and discontinue the plasma etch upon detecting a endpoint signaling change in the bias compensation voltage.

Since Cain discloses that plasma etcher using endpoint monitoring apparatus sensitive to parameters such as DC bias level may be used to implement the etching process (dielectric etching process) (col 8, lines 56-60), one skilled in the art would have found it obvious to modify Cain method by using the endpoint method as taught per Gabriel since Gabriel states that his invention detects imminent endpoint when plasma

etching dielectrics thereby permitting the process to be terminated before the substrate is damaged (col 2, lines 58-60).

Regarding claims 17, 20, Cain discloses that the endpoint signal is generated upon completing etching (col 8, lines 37-40). Fig. 5E shows the etching exposes a portion/gate structure 210 under the contact hole 242.

The limitation of claim 18 has been discussed above.

Regarding claim 19, Cain also discloses forming a TEOS (tetraethylorthosilicate) layer 402 over the surface of the substrate 206 (col 7, lines 39-40), fig. 5C shows that layer 402 is formed between dielectric layer 410 (BPSG) and the substrate surface, which reads on forming an interlevel dielectric layer 402.

### ***Response to Arguments***

5. Applicant's arguments filed 7/7/2003 have been fully considered but they are not persuasive.

Applicants argue that Cain does not teach forming the dielectric layer directly over the surface of the substrate because Cain deposits the dielectric layer 344 over the sacrificial stop layer 340 as shown in fig. 3C. This argument is unpersuasive because although it is true that fig. 3C of Cain shows the dielectric layer 344 is deposited over the sacrificial stop layer 340, fig. 3C also clearly shows that the dielectric layer 344 is formed over the stop layer 340 and the surface of the substrate 306. Thus, the examiner asserts that Cain discloses the step of forming the dielectric layer directly over the surface of the substrate as recited in claims 1, 6, 16 and 21.

Applicant's argument that Cain does not teach or suggest using a bias compensation endpoint detection method because Cain suggests using optical emission method to detect the endpoint of the dielectric layer. This argument is not found persuasive because as recited in col 8, lines 56-59 of Cain, Cain discloses employing endpoint monitoring apparatus sensitive to parameter such as the DC bias level of the plasma rather than the light intensity. Hence, the examiner asserts that Cain suggests using a bias endpoint detection method.

It is also argued that Cain does not disclose etching the IDL result in exposing of a portion of the surface of the substrate. The examiner disagrees because as depicted in Fig. 6F, a contact/opening is shown etched through dielectric layer 510 exposing the surface of the substrate at the bottom of the contact.

In response to applicant's argument that there is no suggestion to combine the references of Cain and Gabriel because modifying Cain using the teaching of Gabriel would add several additional stages to the etch process, the examiner notes that the open claim language of " the method comprising", as recited in claims 1, 6, 16 and 21, does not exclude the use of additional steps in the claimed method.

**6. THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

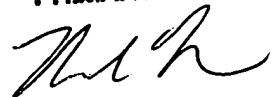
***Conclusion***

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lan Vinh whose telephone number is 703 305-6302. The examiner can normally be reached on M-F 8:30-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on 703 305-2667. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703 308-0661.

NADINE G. NORTON  
PRIMARY EXAMINER



LV  
August 29, 2003